Remarks

Claims 1-11 remain in this application and stand rejected following the Official action of June 13, 2006. Applicants have carefully reviewed the rejections and traverse them for the reasons given below.

Before proceeding to address the rejections, applicants will briefly summarize their invention to assist the examiner in better appreciating the differences between applicants' invention and the art of record. As recited in original claim 1, applicants have provided a media area network that has a storage system including at least one storage device for storing digitized information. A host system provides overall control of the media area network. A host bus adapter connects the host system and storage system. The bus adapter includes a port driver that monitors communications between the storage system and the host bus adapter through an active port, and switches to an alternative port in real time in the event of a failure. Allocating the responsibility for fail-over recovery to the port driver assures timely handling of port failures, thereby reducing potential latency delays.

AMENDMENT TO THE DRAWINGS

Applicants request amendment to FIG. 1 to specifically reference the ports and links described in their specification at Pages 3 and 4. Applicants have also amended the specification to assure correspondence with the amendments to the drawings. Ample support for the amendments exists in the specification as filed at pages 3 and 4 so applicants have added no new matter.

35 U.S.C. 102(e) Rejection of Claims 6-10

Claim 6-10 stand rejected under 35 U.S.C. 102(e) as anticipated by U.S. Patent Application Publication No. 2003/0126315, published July 3, 2003, from an application in the name of Choon-Seng Tan et al., filed December 28, 2001. In rejecting applicants' claims, the examiner contends that Tan et al discloses a storage system having a storage device for storing digitized data, as well as a host system that includes a host bus adapter. Additionally, the examiner alleges that Tan et al. monitor the communication status between the storage system and host bus driver

via a port driver. In the event of a failure, the port driver initiates switching to accomplish fail-over recovery.

Applicants take issue with the examiner's characterization of the Tan et al. patent as teaching all of the features of claim 6-10. In particular, applicants take issue with the examiner's contention that the Tan et al. patent teaches the following features of claim 6:

> monitoring, at a ***lower-level port driver*** (emphasis added) in the host bus adapter, communication status between the storage system and the host bus adapter, and in the event of a failure;
>
> initiating switching ***at the lower-level port driver*** to activate an alternative port, thereby achieving fail-over recovery.

The published application of Tan et al. concerns a network that having at least one storage system (180) connected to at least one host system (150). At paragraph [19], Tan et al. disclose that each host system includes a failover mechanism (134, 164) that acts according to a set of rules to initiate a failover operation. As discussed at paragraph [39] of Tan et al. failover recovery can occur under the following circumstances:

> (1) in a static load balancing environment, only when a preferred path is not aligned with an active controller; (2) whenever a link failure is detected; (3) when an active controller fails to respond; and (4) when a command timeout is received and concurrently path verification has failed.

Nowhere in their patent do Tan et al. perform applicants' monitoring and switching at a lower a lower level port driver. At best, Tan et al. suggest that the failover mechanisms operate at the CPU level [paragraph 21], the very problem applicants seek to avoid by accomplishing monitoring and switching at the port driver level. As discussed at applicants' specification at pages 1 and 2, conventional storage networks, such as that disclosed by Tan et al., which perform the monitoring and switching at a high level, (i.e., the CPU level), incur significant latencies as the commands propagate through the system. Applicants overcome this disadvantage by performing the monitoring and switch at the port driver level. There is no disclosure of suggestion in Tan et al. of performing the monitoring and switching at the port driver level (i.e., at the level of the I/O ports 204 and 208 of FIG 3). The failure of Tan et al. to suggest such monitoring and switching at the port driver level

thus renders applicants' claims 6, and claims 7-10 that depend therefrom, non-anticipated and patentable over this reference. Applicants respectfully request withdrawal of the 35 U.S.C. 102(e) rejection of claims 6-10.

35 U.S.C. 103(a) Rejection of Claims 1-5

Claims 1-5 stand rejected under 35 U.S.C. 103(a) as obvious over the Tan et al. published patent application, as discussed in connection with the 35 U.S.C. 102(e) rejection of claims 6-10, in view of the of the definition of *real time* provided in the Microsoft Computer Dictionary. In rejecting claim 1, the examiner contends that the examiner contends that Tan et al discloses a storage system having a storage device for storing digitized data, as well as a host system having a host bus adapter. Additionally, the examiner alleges that Tan et al. monitor, the communication status between the storage system and host bus driver via a port driver. In the event of a failure, the port driver initiates switching to accomplish fail-over recovery. While the examiner acknowledges that Tan et al. does not specifically disclose performing failover recovery in real time, the examiner suggests that it would have been obvious, in view of the definition of *real time* provided in the Microsoft Computer Dictionary, to perform failover recovery in real time.

Applicants respectfully traverse the rejection of claims 1-5 for much the same reasons as advanced for the patentability of claims 6-10. As discussed above, Tan et al. do not perform applicants' monitoring and switching steps switching at a lower a lower level port driver. At best, Tan et al. suggest that the failover mechanisms operate at the CPU level [paragraph 21], the very problem applicants seek to avoid by accomplishing monitoring and switching at the port driver level. Performing the monitoring and switching at a high level, (i.e., the CPU level), as suggested by Tan et al. incurs significant latencies as the commands propagate through the system. Applicants overcome this disadvantage by performing the monitoring and switch at the port driver level.

Indeed, the ability of applicants' system to switch in *real time*, i.e. the ability to switch with very little latency, readily distinguishes claims 1-5 over Tan et al. Given that Tan et al. do not possess any mechanism for monitoring and switching at the port driver level, a latency will likely exist, thus teaching away from *real time* failure recovery, that is, failover recovery within the same time frame as a failure. For this reason, applicants' claim 1, and claims 2-5 which depend therefrom, patentably

distinguish over the art of record. Applicants respectfully request withdrawal of the 35 U.S.C. 103(a) rejection of claims 1-5.

Objection to Claim 11

Applicants acknowledge the examiner's willingness to allow claim 11 if re-written in independent form. Claim depends from claim 6, which as argued above, patentably distinguishes over the art of record. Accordingly, claim 11 depends from an allowable base claim. Applicants reserve the right to re-write claim 11 at a later time.

Conclusion

In view of the foregoing amendments to the claims and the accompany remarks, applicants solicit entry of this amendment and allowance of the claims. If, however, the Examiner believes such action cannot be taken, the Examiner is invited to contact the applicant's attorney at (609) 734-6820, so that a mutually convenient date and time for a telephonic interview may be scheduled.

Kindly charge the cost of the additional independent claim, as well as any other fees that may be due, to Deposit Account **07-0832.**

Respectfully submitted,
Niall Seamus McDonnell et al.

By: Robert B. Levy
Reg. No. 28,234
Phone (609) 734-6820

Patent Operations
Thomson Licensing, Inc.
P.O. Box 5312
Princeton, New Jersey 08543-5312
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time-out

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An interrupt signal generated by a program or device that has waited a certain length of time for some input but has not received it. Many programs perform time-outs so that the program does not sit idle waiting for input that may never come. For example, automatic bank-teller machines perform a time-out if you do not enter your password quickly enough.

Also spelled *timeout*.